Amendments to the Specification:

Please replace the title on page 1, line 1 as follows:

- Cascaded Charge Pump Power Supply With Different Gate Oxide Thickness Transistors -

Please replace paragraph [0046] with the following amended paragraph:

[0046] Non-overlapping clock signal generator 500 receives as inputs an input clock signal CLK from a system clock input node (not shown) through inverter 510 and an input supply voltage Vdd through PFET 690, PFET 710 and transmission gate 670. Transmission gate 670 comprises two transistors, NFET 735 and PFET 730, configured in the following manner. NFET 735 has its source terminal coupled to the drain terminal of PFET 730, and has its drain terminal coupled to the source terminal of PFET 730. The gate terminal of NFET 735 receives input supply voltage Vdd, while the gate terminal of PFET 730 is coupled to ground.

Please replace paragraph [0047] with the following amended paragraph:

[0047] A clock input stage is formed by inverter ~~Inverter~~ 510 ~~is~~ coupled to transmission gate 670 and inverter 520. Transmission gate 670 provides an input to NAND gate 530, while inverter 520 provides an input to NAND gate 570. The output of NAND gate 530 is transmitted through inverter 540, resistor 600 and inverter 620 to one input terminal of NAND gate 570. NAND gate 570 is similarly configured, such that the output of NAND gate 570 is transmitted through inverter 580, resistor 610 and inverter 630 to one input terminal of NAND gate 530. The cross-coupled NAND gates form a latch coupled to the clock input stage. As such, the cross-coupled connection between NAND gates 530 and 570 ensures that the two clock signal outputs PHI1 and PHI2 will be non-overlapping clock signals.

Please replace paragraph [0049] with the following amended paragraph:

[0049] A clock output driving stage is formed by a pair of NFETS 680, 700 and a pair of PFETS 690, 710. The NFET 680 has its gate terminal coupled to the output of inverter 540, its source terminal coupled to ground, and its drain terminal coupled to the drain terminal of PFET 710. NFET 700 has its gate terminal coupled to the output of inverter 580, its source terminal coupled to ground, and its drain terminal coupled to the drain terminal of PFET 690. PFET 690 has its gate terminal coupled to the output of inverter 550, its source terminal coupled to input supply voltage Vdd, and its drain terminal coupled to the drain terminals of NFET 700 and NFET 720. PFET 710 has its gate terminal coupled to the output of inverter 590, its source terminal coupled to input supply voltage Vdd, and its drain terminal coupled to the drain terminal of NFET 680 and the source terminal of NFET 720. The gate terminal of NFET 720 receives the output of AND gate 560. Clock signals PHI1 and PHI2 are provided at Node 1 and Node 2.

Please replace paragraph [0050] with the following amended paragraph:

[0050] FIG. 6B is a timing diagram depicting the waveforms generated at various nodes of the non-overlapping clock signal generator 500 during operation. As can be seen from FIG. 6A, node A (not shown in FIG. 6B) represents the output of inverter 510. Nodes B and C represent one input of the two-input NAND gates 530 and 570, respectively. Nodes D and E represent the outputs of NAND gates 530 and 570, respectively and are complementary signals which when passed though their respective inverters 540 and 580, may be termed complementary latch outputs. Nodes H and I may be termed intermediate latch outputs and represent the inputs of OR gate 660. Nodes J and K represent the second input of the two-input NAND gates 530 and 570, respectively. Node L represents the output of OR gate 660, while nodes M and N drive the gate terminals of transistors 690 and 710, respectively. FIG. 6B also depicts the system clock CLK, the equalization pulse EQ, and the generated clock signals PHI1 and PHI2.